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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,518	06/03/2005	Robertus Theodorus Franciscus Van Schaijk	BE02 0039 US	3563

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NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
09/07/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/537,518	VAN SCHAIJK ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 6-10* is/are rejected.

7)☒ Claim(s) *3 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

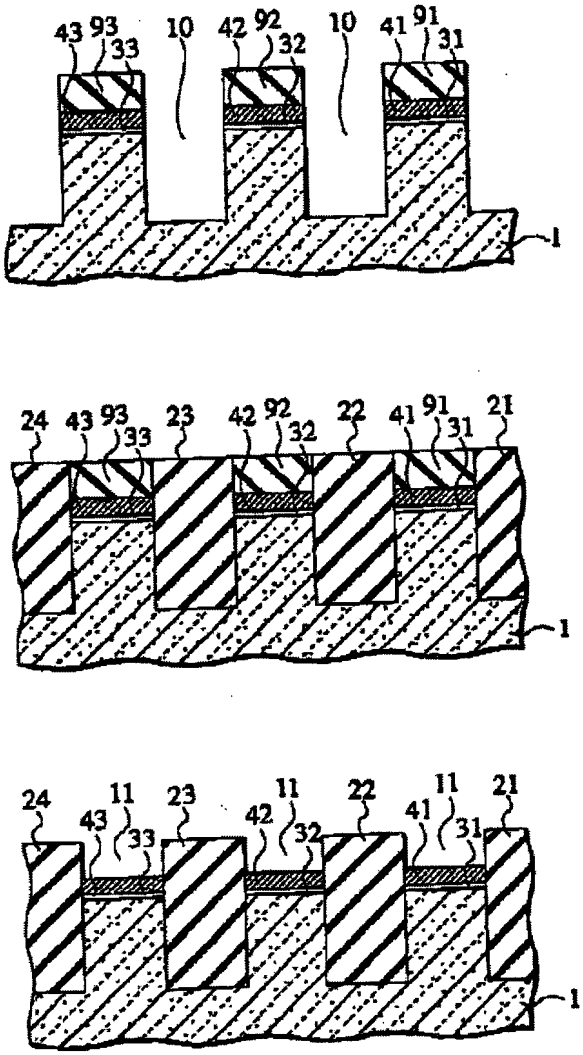
Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4 and 6-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Mori et al., U.S. Patent Application Publication 2002/0093073.

3. Mori discloses a semiconductor process as claimed. See **FIGS. 1A-23D**, where Mori teaches the following limitations.



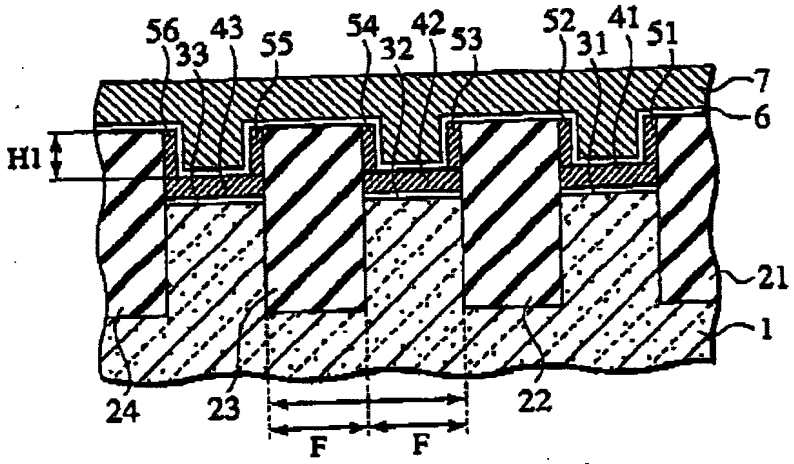
4. Pertaining to claim 1, Mori teaches a method for manufacturing a floating gate type semiconductor device on a substrate having a surface, the method comprising:

forming, on the substrate surface **1**, a stack comprising an insulating film **31,32** and **33**, a first layer of floating gate material **41**, **42** and **43** and a layer of sacrificial material **91**, **92** and **93**

forming at least one isolation zone **21**, **22**, **23** and **24** through the stack and into the substrate,

the first layer of floating gate material thereby having a top surface and sidewalls,

removing the sacrificial material **91**, thus leaving a cavity defined by the isolation zones and the top surface of the first layer of floating gate material, and filling the cavity with a second layer of floating gate material **51**, **52**, **53**, **54**, the first layer of floating gate material and the second layer of floating gate material thus forming together a floating gate.



5. Pertaining to claim 2, Mori teaches a method according to claim 1, further more comprising, after filling the cavity, partially removing the isolation zones so as to expose part of the sidewalls of the floating gate (see FIG. 8A).

6. Pertaining to claim 3, Mori teaches a method according to claim 2,

7. Pertaining to claim 4, Mori teaches the method according to claim 1, furthermore comprising the step of forming a control gate and an interlayer dielectric between the floating gate and the control gate.

8. Pertaining to claim 6, Mori teaches the method according to claim 1, wherein the sacrificial material is any of a nitride layer, an oxide layer or a silicon carbide layer (please note that the instant material is a silicon nitride see [0052]).

9. Pertaining to claim 7, Mori teaches the method according to claim 1, further comprising , after filling the cavity, removing floating gate material present outside the cavity (please note that Mori removes portions of the second floating gate material).

10. Pertaining to claim 8, Mori teaches the method according to claim 1, wherein the first layer of floating gate material and the second layer of floating gate material are the same material.

11. Pertaining to claim 9, Mori teaches a floating gate type semiconductor device, comprising:

a substrate having a surface,

a stack of layers on the surface comprising an insulating film, a first layer of floating gate material, and

a second layer of separately deposited floating gate material on said first layer of floating gate material, the first and second layers forming together a floating gate.

12. Pertaining to claim 10, Mori teaches a non-volatile memory including the semiconductor device according to claim 9.

Objections

13. Claims 3 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

W. David Coleman
Primary Examiner
Art Unit 2823

WDC